

MOS FIELD EFFECT TRANSISTOR 2SJ606

SWITCHING P-CHANNEL POWER MOS FET INDUSTRIAL USE

DESCRIPTION

The 2SJ606 is P-channel MOS Field Effect Transistor designed for high current switching applications.

FEATURES

- Super low on-state resistance:
 $R_{DS(on)1} = 15 \text{ m}\Omega \text{ MAX. (} V_{GS} = -10 \text{ V, } I_D = -42 \text{ A)}$
 $R_{DS(on)2} = 23 \text{ m}\Omega \text{ MAX. (} V_{GS} = -4.0 \text{ V, } I_D = -42 \text{ A)}$
- Low C_{iss} : $C_{iss} = 4800 \text{ pF TYP.}$
- Built-in gate protection diode

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	-60	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	∓ 20	V
Drain Current (DC) ($T_C = 25^\circ\text{C}$)	$I_{D(DC)}$	∓ 83	A
Drain Current (pulse) ^{Note1}	$I_{D(pulse)}$	∓ 300	A
Total Power Dissipation ($T_C = 25^\circ\text{C}$)	P_T	120	W
Total Power Dissipation ($T_A = 25^\circ\text{C}$)	P_T	1.5	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$
Single Avalanche Current ^{Note2}	I_{AS}	-40	A
Single Avalanche Energy ^{Note2}	E_{AS}	160	mJ

Notes 1. $PW \leq 10 \mu\text{s}$, Duty cycle $\leq 1\%$

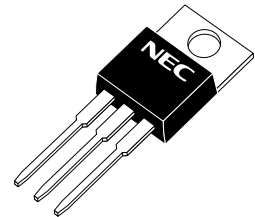
2. Starting $T_{ch} = 25^\circ\text{C}$, $R_G = 25 \Omega$, $V_{GS} = -20 \text{ V} \rightarrow 0 \text{ V}$

ORDERING INFORMATION

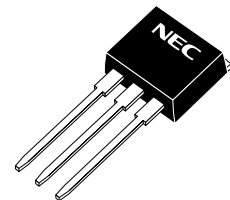
PART NUMBER	PACKAGE
2SJ606	TO-220AB
2SJ606-S	TO-262
2SJ606-ZJ	TO-263
2SJ606-Z	TO-220SMD ^{Note}

Note TO-220SMD package is produced only in Japan.

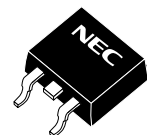
(TO-220AB)



(TO-262)



(TO-263, TO-220SMD)

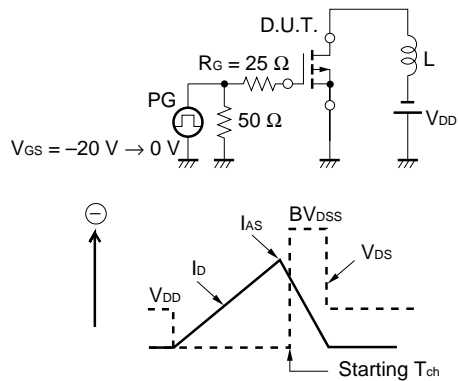


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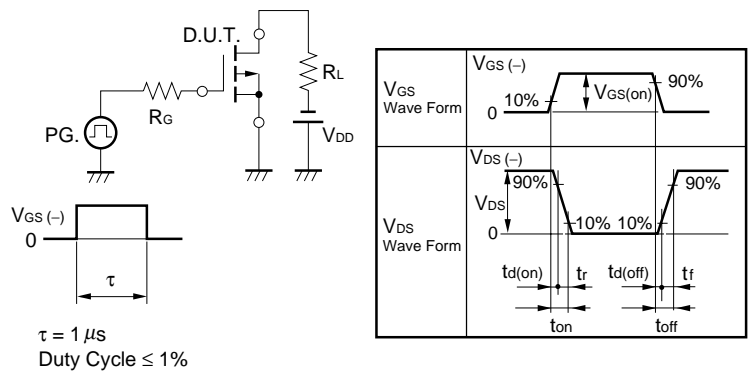
ELECTRICAL CHARACTERISTICS (T_A = 25°C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -60 V, V _{GS} = 0 V			-10	μA
Gate Leakage Current	I _{GSS}	V _{GS} = ± 20 V, V _{DS} = 0 V			± 10	μA
Gate Cut-off Voltage	V _{GS(off)}	V _{DS} = -10 V, I _D = -1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance	y _{fs}	V _{DS} = -10 V, I _D = -42 A	38	74		S
Drain to Source On-state Resistance	R _{DS(on)1}	V _{GS} = -10 V, I _D = -42 A		12	15	mΩ
	R _{DS(on)2}	V _{GS} = -4.0 V, I _D = -42 A		16	23	mΩ
Input Capacitance	C _{iss}	V _{DS} = -10 V, V _{GS} = 0 V, f = 1 MHz		4800		pF
Output Capacitance	C _{oss}			1200		pF
Reverse Transfer Capacitance	C _{rss}			340		pF
Turn-on Delay Time	t _{d(on)}	I _D = -42 A, V _{GS(on)} = -10 V, V _{DD} = -30 V, R _G = 0 Ω		13		ns
Rise Time	t _r			13		ns
Turn-off Delay Time	t _{d(off)}			290		ns
Fall Time	t _f			160		ns
Total Gate Charge	Q _G		I _D = -83 A, V _{DD} = -48 V, V _{GS} = -10 V		120	
Gate to Source Charge	Q _{GS}			20		nC
Gate to Drain Charge	Q _{GD}			30		nC
Body Diode Forward Voltage	V _{F(S-D)}	I _F = -83 A, V _{GS} = 0 V		1.1		V
Reverse Recovery Time	t _{rr}	I _F = -83 A, V _{GS} = 0 V		60		ns
Reverse Recovery Charge	Q _{rr}		di/dt = -100 A/μs		120	

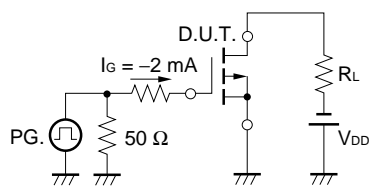
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

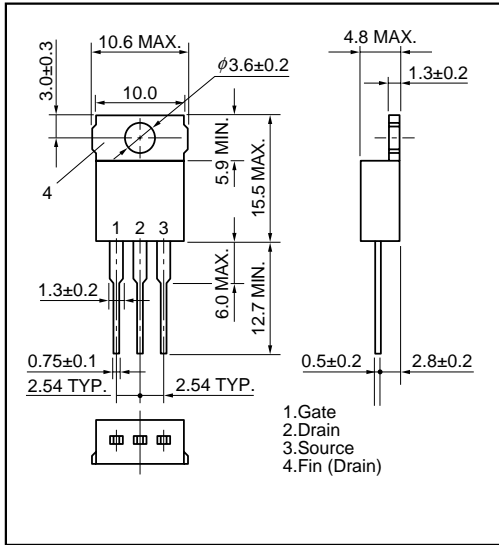


TEST CIRCUIT 3 GATE CHARGE

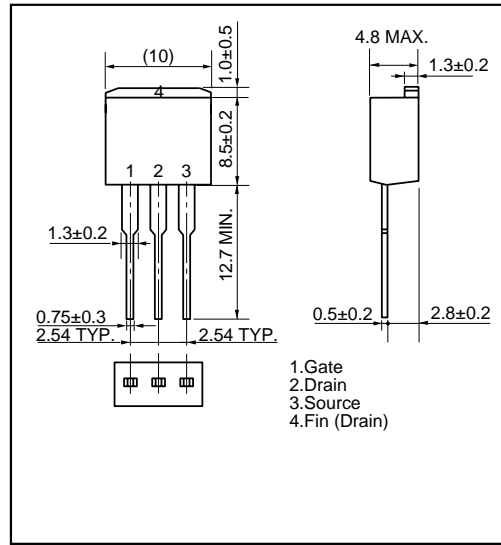


PACKAGE DRAWINGS (Unit: mm)

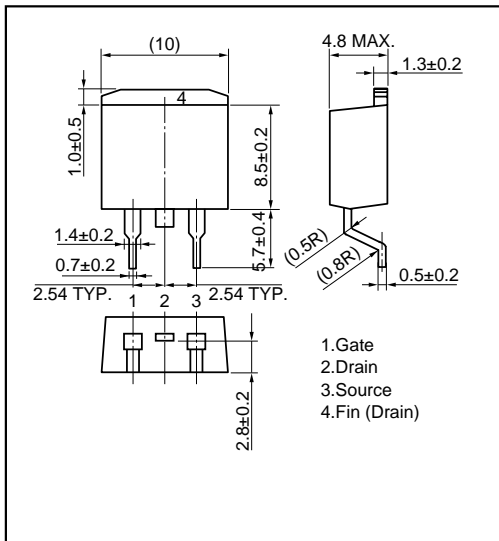
1) TO-220AB(MP-25)



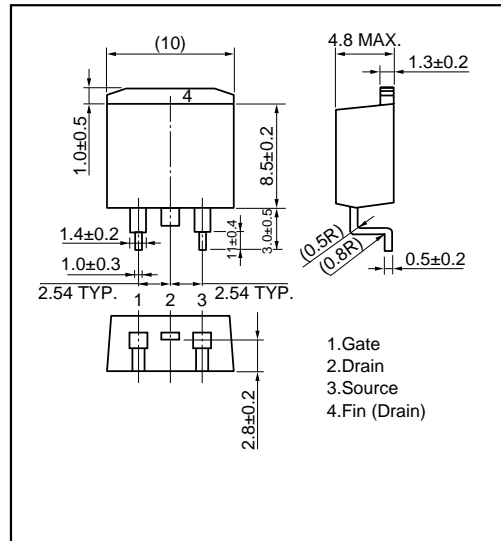
2) TO-262(MP-25 Fin Cut)



3) TO-263 (MP-25ZJ)

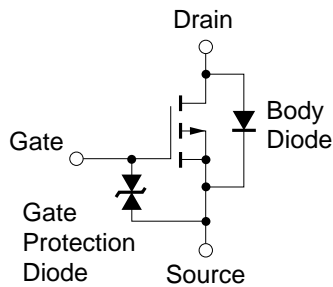


4) TO-220SMD(MP-25Z)^{Note}



Note This Package is produced only in Japan.

EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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